Through-Wafer Trench-Isolated Electrical Interconnects for CMUT Arrays

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***Abstract*–Through-wafer trench-isolated interconnects provide electrical access to elements in a capacitive micromachined ultrasonic transducer (CMUT) array. The series resistance of these interconnects is low (4.5 Ω), and the element-to-element electrical crosstalk is insignificant (less than -53 dB at 5 MHz). This interconnect technique is compatible with both surface-micromachined and wafer-bonded CMUTs. Compared with the existing through-wafer via interconnect process, through-wafer trench isolation can be achieved by a simpler fabrication process and enables the implementation of curved CMUT arrays.**

***Key words* – CMUT; through-wafer trench-isolated interconnect; curved CMUT arrays**

I. INTRODUCTION

2-D ultrasonic transducer arrays are needed for next-generation real-time 3-D ultrasound imaging systems. The CMUT technology is a promising candidate for making 2-D arrays for such systems because of the combination of the low-cost micromachining process and demonstrated performance advantages [1, 2]. The existing interconnect scheme in 2-D CMUT arrays is based on through-wafer vias [3]. In this implementation, high aspect ratio vias are etched from both sides of a silicon wafer using deep reactive ion etching (DRIE), and later filled with conductive materials such as doped polysilicon. CMUTs are fabricated on the front side of the silicon wafer, and bond pads are formed on the back side. However, residual stress, surface contamination, and roughness caused by the through-wafer via process complicate its use with the silicon-on-insulator (SOI) wafer-bonding CMUT fabrication technique, which requires a clean and smooth wafer surface. SOI wafer-bonded CMUTs have higher fill factor and better process control when compared to the surface-micromachined CMUTs [4].

This paper introduces a novel method that provides interconnects to individual elements in a CMUT array. CMUT membranes are prefabricated on the front side of a silicon wafer. Deep trenches are then etched from the back side into the highly conductive silicon substrate to isolate the elements and create silicon pillars that form signal electrodes of the membranes. This technique significantly reduces process complexity and is compatible with both surface-micromachined and SOI wafer-bonded CMUTs. Additional advantages include reduced series resistance, low element-to-element electrical crosstalk, and the possibility of implementing flexible CMUT arrays.

II. FABRICATION PROCESS

In this study, 2-D (16-element x 16-element) CMUT arrays with trench-isolated interconnects were fabricated. Table I summarizes the device parameters of the fabricated arrays. These arrays have a 250-μm element pitch and a trench width of 15 μm. The final silicon substrate was 120 μm, thinned down from a standard thickness of 500 μm.

TABLE I: DEVICE PARAMETERS OF THE TRENCH-ISOLATED CMUT ARRAY.

Membrane Width (μm)	48
Membrane Length (μm)	220
Number of Membranes / Element	4
Membrane Thickness (μm)	2.56
Cavity Height (μm)	0.3
Substrate Thickness (μm)	120
Trench Width (μm)	15
Element Pitch (μm)	250
Silicon Wafer Resistivity (Ω-cm)	0.025
Riston Film Thickness (μm)	15

The through-wafer trench-isolated CMUT fabrication starts with the formation of CMUT membranes on the front side of the wafer. The CMUT membranes can be fabricated using either silicon nitride surface-micromachining technology or SOI wafer-bonding technology. The wafer-bonding technology was used in this study.

Fig. 1 shows the fabrication steps. Using the SOI wafer-bonding technique, CMUT membranes are fabricated on the front side of a highly conductive silicon wafer. The wafer front side is then temporarily bonded to a quartz carrier wafer, which provides mechanical support and optical transparency for later processing steps. A 15 μm thick dry photo resist film (Riston CM206, Dupont, Wilmington, DE) is used as the bonding adhesive. The dry photo resist film provides good adhesion, uniform thickness across the wafer, and reduces bubble formation and out-gassing during subsequent etching and metallization steps in high vacuum conditions. The silicon substrate is thinned down to 120 μm

by mechanical grinding and polishing. This step reduces the subsequent DRIE time, improves the trench profiles, and decreases the series electrical resistance and cross coupling capacitance of the interconnects. The silicon wafer can be thinned down to other desired thicknesses so that the interference due to the substrate reverberation is pushed out of the operation frequency band of the CMUT.

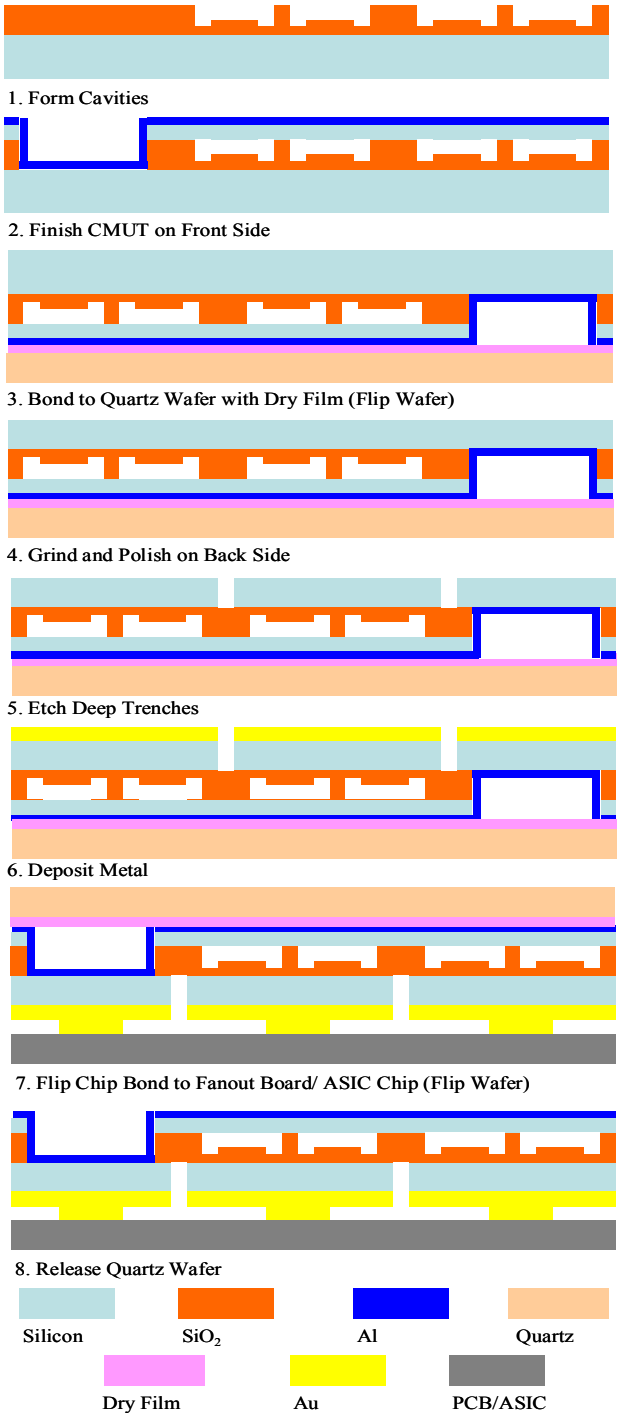


Figure 1: Fabrication steps for through-wafer trench-isolated CMUT arrays.

Through-wafer trenches are etched into the substrate from the back side using DRIE. A Ti/Cu/Au layer is then evaporated to form the metallization on the signal electrodes. The evaporation is performed at an oblique angle to prevent electrical shorting between neighboring pillars. This also eliminates the need for an additional lithography step to define the signal electrodes. Fig. 2 (a) shows a back side view of 12 trench-isolated elements after the metallization step. The wafer is then diced to separate individual devices. The arrays are flip-chip bonded to a fan-out board or an integrated circuit (IC) chip using anisotropic conductive film (ACF). Other flip-chip bonding techniques such as eutectic solder bumping can also be used. After flip-chip bonding, mechanical support for the array elements is provided by the fan-out board or IC chip. The quartz carrier wafer can then be safely released. Fig. 2 (b) and (c) show 12 CMUT membranes after releasing the quartz wafer and a trench profile respectively. The surface profile of the CMUT after the carrier wafer is released is taken by a Zygo surface profiler (Model NewView 200, Zygo Corporation, Middlefield, CT) [Fig. 2 (d)]. In this measurement, the array is bonded to a flat substrate before the quartz carrier is released, resulting in a smooth and flat surface on the CMUT front side.

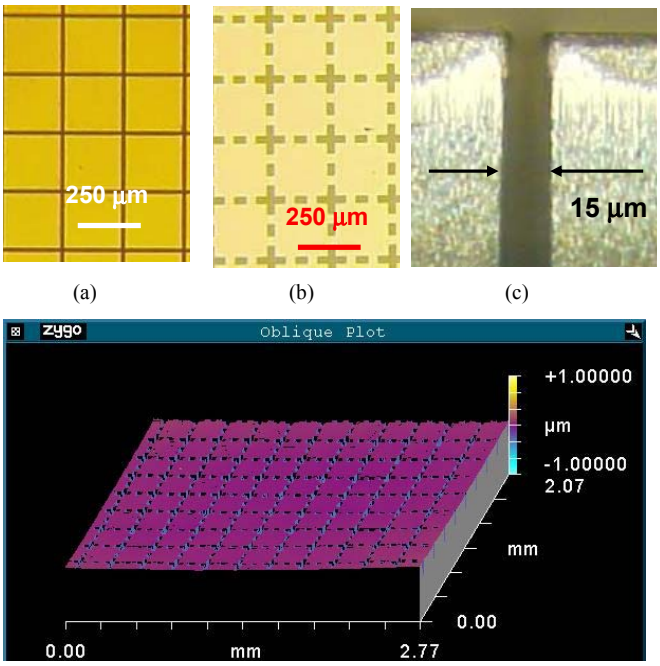


Figure 2: (a) Back side of silicon wafer after trenches are etched and metal is evaporated; (b) front side of wafer after releasing quartz carrier; (c) trench profile; (d) optical surface profile of an array of elements.

The through-wafer trench-isolated interconnect scheme is a two-mask process, which is significantly less complex than the existing through-wafer via interconnect scheme which is a six-mask process, and includes long oxidations, depositions, doping and etching steps.

III. TEST RESULTS

A network analyzer (Model 8751, Hewlett-Packard Company, Palo Alto, CA) was used to measure the input impedance of the trench-isolated CMUT elements. Simulations based on an equivalent circuit model [5] were also performed. Fig. 3 shows a comparison and a good fit between the predicted and measured electrical input impedances of a CMUT element at a bias voltage of 110 V. Using the same setup, the collapse voltage was determined by increasing the bias voltage until the fundamental resonant frequency (as shown in Fig. 3) disappears, which was found to be 175 V (reasonably close to the predicted value of 180V) for this CMUT element.

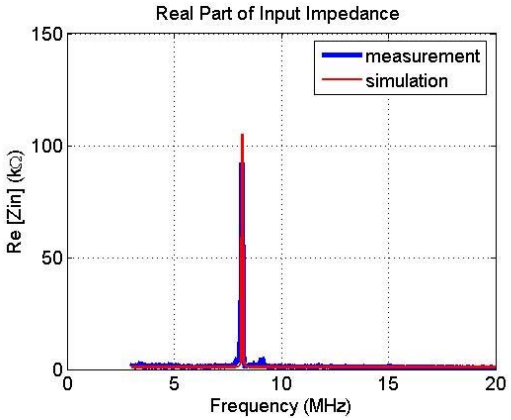


Figure 3: Real part of input impedance of trench-isolated element in air.

In another measurement, a custom designed IC [1] which contains transmit/receive circuitry was used to determine the resonant frequency of the CMUT elements in air. The resonant frequency at a bias voltage of 40 V (Fig. 4) has a uniform distribution over 100 randomly selected elements, with an average resonant frequency of 8.52 MHz, and a standard deviation of 0.1 MHz.

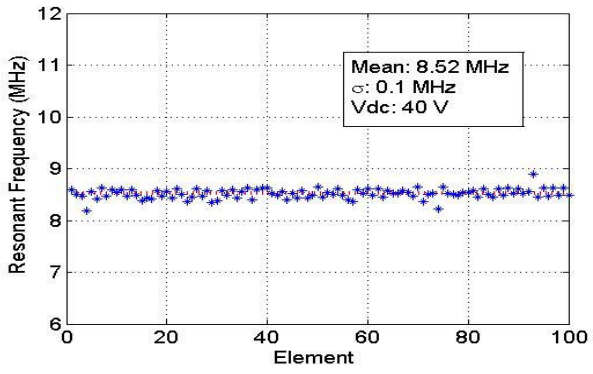


Figure 4: Resonant frequency distribution.

The real part of the input impedance at 20 MHz was extracted from the input impedance measurements to determine the total series resistance. At this frequency, the real part of the CMUT impedance is negligible. Since the aluminum traces on the fan-out board have well defined geometries, resistance due to these traces was calculated and subtracted from the total measured resistance, and resistance due to the trench-isolated interconnect and the flip-chip bonds was obtained. Fig. 5 shows the resistance values for 20 randomly selected interconnects. The average resistance is 4.5 Ω, and the standard deviation is 1.8 Ω. A large fraction of the resistance is due to the flip-chip bond resistance. Compared with existing through-wafer via interconnects (which has ~20 Ω resistance), the series resistance is significantly reduced [3].

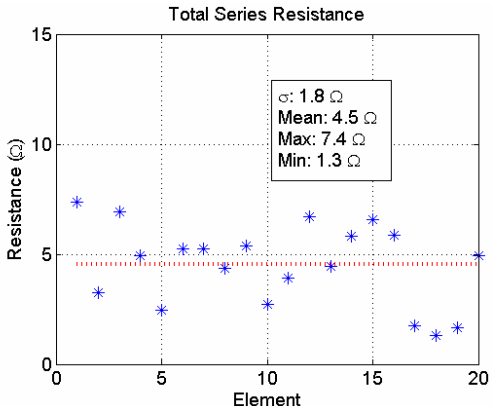


Figure 5: Series resistance distribution.

Element-to-element electrical crosstalk was measured by exciting one element with a 50-ns pulse, and detecting the electrically coupled signal from neighboring elements. Both the excitation and received pulses were measured on a 1-MΩ load. In the worst case where two elements are next to one another (A-B), the electrical crosstalk is less than -53 dB at 5 MHz. Fig. 6 shows the electrical crosstalk spectra. The cross coupling capacitance between two neighboring elements (A-B) is 29 fF. The electrical crosstalk is significantly lower when the termination resistance is 50 Ω.

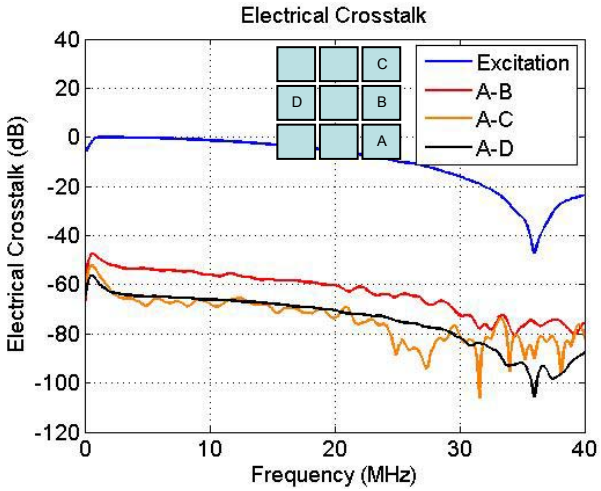
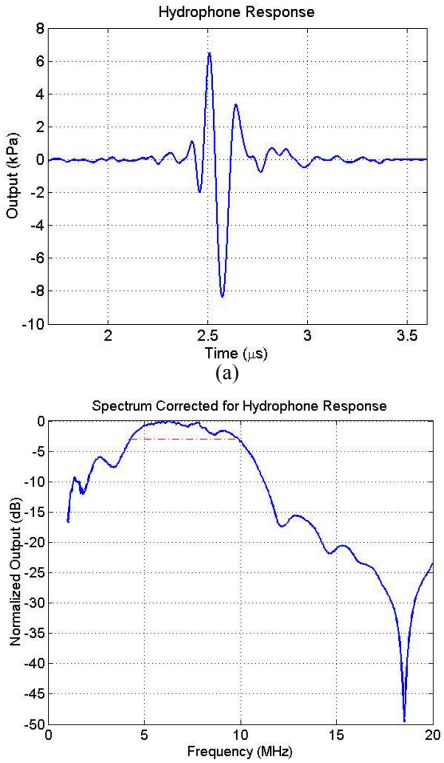


Figure 6: Electrical crosstalk.

Finally, a trench-isolated CMUT array bonded to a fan-out board was tested in immersion. A hydrophone (Model PZT-Z44-0400, ONDA Corp., Sunnyvale, CA) was used to measure the output pressure. The hydrophone was positioned at a distance of 3 mm from the transducer surface. A 17-dB, 10-kHz to 25-MHz, 50-Ω preamplifier was used to amplify the hydrophone signal before it was read into an oscilloscope. The device was biased at 80-V DC. A 30-V unipolar pulse with a pulse width of 100 ns was applied to the device, and the oscilloscope readings were recorded [Fig. 7(a)]. The Fourier transform of the signal measured with the hydrophone, after correcting for the hydrophone frequency response, has a center frequency of 6 MHz, and a 3-dB fractional bandwidth of 80% [Fig. 7(b)].



(a)

(b)

Figure 7: (a) Hydrophone measurement; (b) corresponding spectrum.

IV. DISCUSSIONS

An important feature associated with the trench-isolated interconnect scheme is the capability to implement flexible CMUT arrays. Preliminary results obtained in this study show that it is possible to fold trench-isolated CMUT arrays without breaking the silicon and oxide membranes on the front side of the array. Curved 2-D CMUT arrays are useful in applications such as side-looking catheters and large-area conformal arrays for imaging and therapy. Fig. 8 shows 2-D arrays curved in one direction after the quartz carrier wafer has been released.

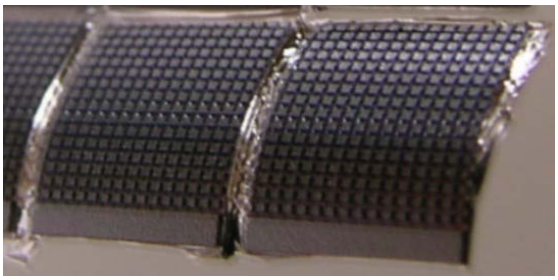


Figure 8: Curved 2-D CMUT arrays.

V. CONCLUSIONS

Through-wafer trench-isolated interconnects for 2-D CMUT arrays are demonstrated. CMUT devices with trench isolations were tested both in air and in immersion. The fabrication process for the new interconnect is simpler than that for the existing through-wafer via interconnect. Since CMUTs are prefabricated before the trenches are etched, this technique can be used regardless of the method used to build the membranes. Trench-isolated interconnects have negligible series resistance and electrical crosstalk. Since the carrier wafer provides additional mechanical support, the device wafer itself can be thinned down to a desired thickness for enhanced acoustic performance as well as improved substrate flexibility. Future work includes the demonstration of this technique with surface-micromachined CMUT arrays and the integration of this interconnect scheme into a real-time 3-D ultrasound imaging system.

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REFERENCES

[1] I. O. Wygant, *et al.*, "An endoscopic ultrasound imaging system based on a two-dimensional CMUT array: real-time imaging results," presented at *2005 IEEE Ultrasonics Symposium,* Rotterdam, The Netherlands, September 19-21, 2005.

[2] D. M. Mills, "Medical imaging with capacitive micromachined ultrasound transducer (CMUT) arrays," *Proc. 2004 IEEE Ultrasonics Symposium,* pp. 384-390, Montréal, Canada, August 24-27, 2004.

[3] C. H. Cheng, E. M. Chow, X. Jin, A. S. Ergun, and B. T. Khuri-Yakub, "An efficient electrical addressing method using through-wafer vias for two-dimensional ultrasonic arrays," *Proc 2000 IEEE Ultrasonics Symposium*, pp. 1179 – 1182.

[4] Y. Huang, A. S. Ergun, E. Haeggstrom, M. H. Badi, and B. T. Khuri-Yakub, "Fabricating capacitive micromachined ultrasonic transducers with wafer-bonding technology," *Journal of Microelectromechanical Systems, 12*, 2003, pp. 128- 137.

[5] W. P. Mason, *Electromechanical Transducers and Wave Filters*. London: Van Nostrand, 1948.