SYSTEMS CONCEPTS 520 THIRD STREET SAN FRANCISCO, CALIFORNIA 94107

March 20, 1978

Received of Systems Concepts the following documents regarding the Systems Concepts Digital Synthesizer:

Specifications (Programming and Analog Output)
Theory of Operation
Wire List (Volumes 1 and 2)
Engineering Drawing Conventions
Engineering Drawings (Volumes 1 and 2)
Diagnostic Programs Manual

(Signed) Kenneth E. Shoemake

TELEPHONE: 415-442-1500 TWX: 910-372-6062

Stanford contracts,

P.O.s,

grant proposals.

Your eyes only.

5.4.2.2. Check hang flag

Actually, the next little bit of code belongs under the heading of "debugging."

```
readWcA1:
        lack    dmem_wcmaHangA1
        nop                             ;       tblw    nextWcmaA1 = 0x7D15
foo:    lack    dmem_wcmaHangA1
        tblr    tmp
        zals    tmp
        bnz     foo
```

In the last three lines, we read the contents of dmem_wcmaHangA1 into the on-chip RAM location given by tmp, then check tmp for 0. As long as dmem_wcmaHangA1 is non-zero, we will loop here.

The key here is the nop. If you replace it with the tblw nextWcmaA1 instruction in the comment field (which assembles to 0x7015 under the current variable assignments), then you are *guaranteed* to have a non-zero dmem_wcmaHangA1. This means that *every time* a new buffer pointer for the current stream is read in, the TMS will hang in this loop; and you have the added luxury of being able to read, in location dmem_wcmaHangA1, where the buffer pointer starts that you're about to read into the TMS. Alternately, you can set dmem_wcmaHangA1 by hand, and the TMS code will hang in this loop the next time that a new buffer pointer is read in for this stream. The code is written so that the looping occurs until you, by hand, set dmem_wcmaHangA1 to 0.

5.4.2.3. Reading in wc and testing it for 0

As discussed in "OIB: The 32010–68000 Software Interface," we must ensure that wc never is 0:

```
readWcA1:
        zals    nextWcmaA1              ; 1
        tblr    wcA1                    ; 2
        zals    wcA1                    ; 3
        bnz     wcA1OK                  ; 4
        lack    dmem_err_wcA1_zero      ; 5
        tblw    nextWcmaA1              ; 6
        b       readWcA1                ; 7
wcA1OK:
```

(In the code, the first label above is of the form readWcXX.)

The first two lines read in wc for the new buffer pointer. Obviously, nextWcmaA1 points to the start of the new buffer pointer, and wcA1 is the on-chip RAM location that will hold the click count for the new buffer in MEM. In line 3, we load that new wcA1 into the AC, and test it in line 4 for 0. For non-zero wcA1, we branch to wcA1OK and go on our merry way.

For wcA1=0, which is an error condition, we fall through and start hanging in a loop. First, we set the DMEM location given by dmem_err_wcA1_zero to the non-zero value equal to nextWcmaA1. The 68000 should occasionally check dmem_err_wcA1_zero; if it goes to non-zero, an error message should be printed out. After the error flag has been set, we loop back to readWcA1:, and continue looping until wc pointed to by nextWcmaA1 is non-zero.

STANFORD UNIVERSITY
PROCUREMENT SERVICES DEPARTMENT

851 Welch Road
PALO ALTO, CALIFORNIA 94304

October 5, 1977

CERTIFIED MAIL

Systems Concepts
524 Second Street
San Francisco, California 94107

Attention: Mr. Peter R. Samson

Subject: Stanford University Purchase Order C 601535

Gentlemen:

Subject Order, dated January 12, 1976, called for delivery of the goods thereunder within 110 days of Order or March 1, 1976, whichever was later. Firm order was accomplished by Change Order No. 1, dated April 16, 1976, removing the originally inserted contingency clause. This had the effect of establishing the delivery date as August 4, 1976.

During the intervening year you have postponed delivery numerous times. Approximately two weeks ago you informed us that delivery would be made by October 7, 1977. We have suffered substantial inconvenience from these delays and cannot tolerate them any further. If acceptable delivery, in full, is not made to Stanford on or before October 14, 1977, then we will consider you in material breach of the above Purchase Order. We therefore may refuse any delivery after October 14, 1977, and hold you liable for any damages suffered by reason of your delays; however, repurchase against your account is not anticipated.

Please advise.

Sincerely,

T. E. Killebrew
Director

bc: Les Earnest/John Chowning

TEK:adv