Systems Concepts Synthesizer

Log #1

LABORATORY NOTEBOOK

Department CCRMA

Stanford University
Stanford, California

Subject Time ordered Log

Date (30 Nov 77)
Time (1544) ENTRY -use ink Initials (KS)

12/9/77 1700 Acceptance clause signed By SC+Stfd DGL
First order of business is for them to fix pending bug in gp term. Presumably, the chess-clock is ticking against them from now until it is fixed.

12/10 1500 Stu Nelson showed up to start poking at gp bug. *

12/10 1645 gp bug seemingly fixed. Ran Amptst, wins. DGL
ampnrp, ampnr1, win,win.

12/19 Reverb up. DGL

12/ 22 ~~Sang~~ Wait + pause + clear wait-pause works. DGL

22 Dec 77 1800 Previously working command list failed, getting hung making nasty sounds. ADFID.DMP was the loser. May be due to massive power glitches (which clobbered KL & 6). KS

12/23 Re above problem: seems to be somewhat (?) dependant on # of commands. Symptoms of lossage seem to indicate ~~that~~ it stops processing updates at some point rather high in the command list. But, it stops in different places even with the same .Dmp file! However, it always stops in roughly the same place, give or take a few ~~milliseconds~~ seconds. Samson box never returns, wenn exausted. DGL

Signed..... Date.....

12/23 Problem put in simple form of 10 note ~~[illegible]~~ scale
17:17 played .1 sec per note (files: Over (score input) Over.dab, Over.dmp.) to play for 100 secs. It only plays to 92 sec. Figuring ~~out where~~ that it is command length dependent, I calculated this to be around absolute addr of '100000 in the six.

Called S.C., talked to Pete, but as it was time for me to leave for vacation, I only described the problem, I did no further debugging. I couldn't tell, for instance if the Box was complaining about NX mem., etc., since it never returned to the rtj. Referred Pete to S.C.

Sighs...

DGL

12/30 RAU simple test (sinusoid with ramped amp) through DLY memory - no failure. Then took out the throw-away delay in complex reverb - no noise!! Must have been 'cause of ~~the~~ grain confusion on comb-filter dly mode. Remember we made that change after other difficulties. S.C.

12/30 Problem with simple additive synthesis. Files TRP1* [SAM, DGL] attempt to generate <u>one</u> note, 12 harms, 5-8 segs per function. Spurious frequencies, attributed to lack of updates. DGL is working on it.

JMG.

Signed Date

1/3 I'm not sure that problem in 12/30 j.e. has been resolved. Seat of pants thing. It's on my list for further poking.
DGL

1/10 16:59 Problem in DMA, box hangs, problem first noted 12/22/77 @ 1500 nailed down, box responding w/ PE + NX errors while hung. Hanging seems to be related to absolute memory (pushing up command list in 6's memory causes it to die sooner). Called Pete @ 16:59.
— DGL

1/11 Moved terminator cards for Samson box port in old Ampex into correct slots. JBR
Replaced W102 in C8 in old Ampex mem JBR

12 Jan 78 23:45 Confirmed hardware bug with generator in sum of cosines mode. File SC1.DAB[SAM,JOS] shows a losing command list. KS/JOS

13 Jan 78 10:50 Samson returned my call at 10:AM - I pointed him to the file - he wanted to know what the effect of changing (increasing) the Sc Factor - and it must for sum of cosines terms. Do we
J.C.

26 Jan 78 1700 Postscript to sum of cosines problem: increasing scale by 2 seems to avoid problem in all tested cases. Not mathematically correct, but appears to stem from lack of post-normalization after $\frac{\sin nx}{\sin x}$ multiply. (Really 13 Jan 78 should be date on this, but prior note wasn't completed.) KS

Signed Date

26 Jan 78
1700
* Started getting ME bugs from intermittent delay memory parity errors. Called Pete Samson and investigated further. Using DMT in Jaxtst failed to show any errors, but MKEXER showed a clear failure on DAC2, which is the output from delay memory. Scoping the signal, it looked like bit 1 of negative samples was being dropped. Pete wanted us to run DMT in JAXTST overnight, said they'd be down to fix it. KS

1900 JC Conversation with Mike L. - they won't come to fix it 'til weekend therefore we ~~[illegible]~~ will DMT tomorrow aft. (Friday) through early eve. to keep out of other users way (use of six) Lewitt agreed.

* 30 Jan 78
2353
Pete and Stu arrived today at ~1400 KS to fix bug. Results so far are that 2 problems resulting in erroneous ME indications have been cleaned up. Unable to pin down

(cont) bit 1 dropping bugs. Symptoms were clear when they first arrived, but powering down to switch cards may have made it go hide. Speculation is that the bug still exists, but is not manifesting itself. No visible bugs as of now. Cards for delay memory data path for bits 0-3 and 4-7 were switched.

31 JAN JC – Stuart arrived ca 2:00 PM to chase parity error bug. Error is still there, although much less frequently. *

31 Jan 78 18:20 KS – Stuart is knocking off for the day. His current hypothesis requires some extra equipment to test. He plans to come down tomorrow with the equipment.

1 Feb 78 18:45 KS – Pete and Stu arrived today (before me) (ca 10:30 AM SC) and started in debugging again. Found a timing bug involving master reset sometimes writing garbage into delay memory, fixed that. Investigation of Julius' & Tovar's complaint about one zero filters not working showed an unambiguous bug. Pete says *

(cont.) that the LØ running term always looked like −∈ (ie, all ones). Also that the cause of the bug was somewhat embarassing. They claim to have fixed that bug.

2 Feb 78
*0300 Still here with Stu Nelson - problem with bad data in ALL PASS REV mode of Modifier still not solved.

0400 Stu cannot find the problem - packing up after a hard night - back at it later today. Julius is happy with fitters following the "fix" "embarassing" said Pete !! J.C 0415

2 Feb 78
19:35 KS — Stu just left, claiming to have found and replaced the chip responsible for reverb clicks and pops. He had already done that once before, but evidence still pointed at that chip. Unfortunately he seems to have munged a chip associated with delay memory, causing a bad bit. He has arranged for that bit to be an inaudible low-order bit until he can return tomorrow and fix it.

2 Feb 78
20:00 KS We played ADFID before Stu left, with no noise audible, as well as TES and other files. However when playing ADFID for Gareth and John only a little later, extreme clicks and pops occurred. This file has never exhibited such symptoms before.

Signed..... Date.....

3 Feb 78
23:30 KS – Maybe this time... Stu claims to have finally found and fixed the real thing. All the sound files I have tried seemed to go thru cleanly, with no clicks and pops. The problem involved the original bit 1 bug, and stemmed from a bad 256x1 memory chip for running terms (L0, L1). This was replaced. No further problems were observed, including the hypothetical munged chip mentioned in my 2 Feb entry.

MAY 14, 1978 DGL – Began picking up ME PE errors in JC's standard reverberator, CHED4[SAM,JC]. Any access of delay memory causes SAMX to get SAM – MINT = 40000 2763421, ie, ME ~~[illegible]~~ is ~~[illegible]~~ on.

For an example prog that does this, R MBOX & feed it CHED4[Sam,DGL].

21 May 1978
14:00 KS – Pete and Stu arrived for debugging session.

20:30 KS – Left. Bug status: 2pole scale loss was our software, interrupt bug postponed, "crosstalk" bug seems to be flakey RAM-supply ~~[illegible]~~ bump; no others failed to appear (delay mem errors, end of buffer blip).

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29 May 1978 KS Stu arrived for hardware fixing.
* 14:30

23:00 KS Talked to Stu on phone after he returned
(entered 30 May 78 14:18) from dinner. Seems to be design problem involving length of signal path from modifier thru delay memory and back to modifier. Stu planned to poke some more then talk to Pete about fix.

1 June 78 JEG
early morning

Error Message:
"Didn't get SAM-MCDONE message, got SAM-MINT/dat=
4000002563421"
Soundresult: "Knack".

5 August 78 KS Pete, Stu, and Mike Levitt arrived around
22:30 1230 to fix loss resulting from Tuesday's wiring
* Sat change (not logged above). Left about 2200 with all known problems fixed (but possible bugs with read data?). Need to clear delay memory thru modifiers to clear internal buffers.

27 September 1978 KS, TED Getting dropped bits in packed read data. Low half of memory drops bit 8, sometimes bit 9; high half drops bit 30. Memory signals look okay at box, but it fails to latch data?

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Also JC wants something done about limit cycles causing buzzes in reverberators at the tail end of decays.

3 December 78 19:45 KS – Traced dropped bit 8 to suspected bad solder joint in memory cable (S.C.'s), which Ted fixed. Seems better now. Charlie Kagell (sp) came down from S.C. on 1 Dec 78 and made wiring change to fix long-standing read-from-adjacent-generators design bug. Seems fixed. At 14:00 today Pete & Stu arrived to check that fix and work on sum memory bugs. Sum memory bugs traced to (more) bad memory chips, replaced them. (Locations around modifier-side '40 and '50.) Investigated write data, found same kind of design bug as with read data; designed and installed fix. All known bugs in synthesizer now appear fixed. Reverb buzz still exists, mostly audible because of -ε's interspersed with 0's, which is particularly rough on DAC's. Suggest avoiding by using small offset (say, ±ε) added to reverb output.

4 Dec 78
5:00

KS — Box dead with dead main power supply! We were getting no response, CONI gave Ø's, checked power (at JBR's suggestion), found no voltage for main supply. Pulled all cards: still dead suppy. Disconnected leads: still dead. Therefore dead supply. Box left off, cards out, power supply partially disconnected. RP did most of dirty work.

12 Dec 78
10:30

KS — Ted poked parity problem (dropped bit 25 in high mem, bit 8 in low), decided S.C.'s cable had too much load. Pete called with hunch that cable was doubly terminated. It was. Ted removed set of terminators on bottom of box, on Pete's suggestion. Fixed it.

Signed ..... Date .....

17 Dec 78
23:15

KS— Weekend update. On Thursday Pete and Stu came and poked ~~Turenas~~ read data problems, particularly ~~reverberated explosions~~ picked bits 2000. These were traced to interference from diagnostic readback thrashing when address Ø was selected (the default). A software fix was proposed and installed in the SIXSYS to set the default kludged in value from the data switches to 177. Today we discovered that Tovar's SAMPLA did not include the data switch kludge (not surprisingly), and adapted our fix accordingly to kludge in switches unless 2 bit is set in CONDA. Kludged value is 177 unless left of switches is 105 (random magic number). Turenas was having commands munged by the same mechanism that caused read data lossage. Yesterday (Sat.) was devoted to Turenas problems, particularly reverberated explosions. These were traced to extremely noisy carry lines (FCC) in

(cont.)

Signed Date

(cont) the modifier multipliers. The reason for the noise is still unknown, but terminating the lines gave a temporary fix. Looked at that again today, but still no real fix. Discovered some potential software problems while poking today, one being that STIFLE failed to clear GO's, the other that BoxAss's optimizing makes false assumptions so that reordered commands could lose. Diagnostic read back problem still needs a real hardware fix. One problem remains unsolved in Turenas: using SAMPLA it wins but XSAM/SAM/SAMX get bumps at junctures of the space function.

25 Mar 79 1930 KS — (entered 27 Mar 79) Pete & Stu arrived at 1430 to fix "rebroken" infinite bad interrupt bug. Previous wiring change for this bug attacked correct basic timing problem generating bug, but did not provide sufficient margin. More hardware

(cont.) mods were made to improve margins. Seems okay now — no bad interrupts recorded. Next, an attempt was made to further investigate the noisy lines mentioned in previous log entry. Conclusion was that "lines are just noisy....", and pull-up resistors were left as the best fix.

Signed Date